# INDIA

## SEMICONDUCTOR TALENT

## INTELLIGENCE REPORT

2025–26 Edition

Workforce Scale · Compensation · Competition · Attrition

**Peepal Consulting**

Peepal
20 YEARS OF TRUST

**200K–250K (est.)**
Semiconductor professionals (est. range)

**$45–50B**
India market size (2024–25)

**3,549**
GCC open roles (Q1 FY2026)

**20%**
Global chip-design workforce

**105+**
Design startups under DLI

**5 sections**
Industry · Competition · Talent · Compensation · Workforce

# TABLE OF CONTENTS

# EXECUTIVE SUMMARY

**200K–250K**
Semiconductor professionals in India (2025–26)

**$45–50B**
India market size (2024–25)

**$100–110B**
Projected market by 2030

**3,549**
GCC open roles (Q1 FY2026)

**-22%**
YoY open positions (demand trough) in design GCCs (Q1)

### DESIGN DOMINANCE

Bengaluru + Hyderabad account for ~65% of chip-design talent (proxy estimate; ~143,000 professionals). Concentration is entrenched — growth is skill-specific (AI/HPC, verification, advanced PD), not uniformly broad.

### MANUFACTURING RAMP

Gujarat (Ahmedabad cluster) and Assam are emerging as the primary fab/ATMP hubs. Micron, TSAT, and CG Power driving demand. Note: capex commitments are now; broad fab-floor hiring is 2–4 years out — near-term roles concentrate in project setup, procurement, process, and facilities.

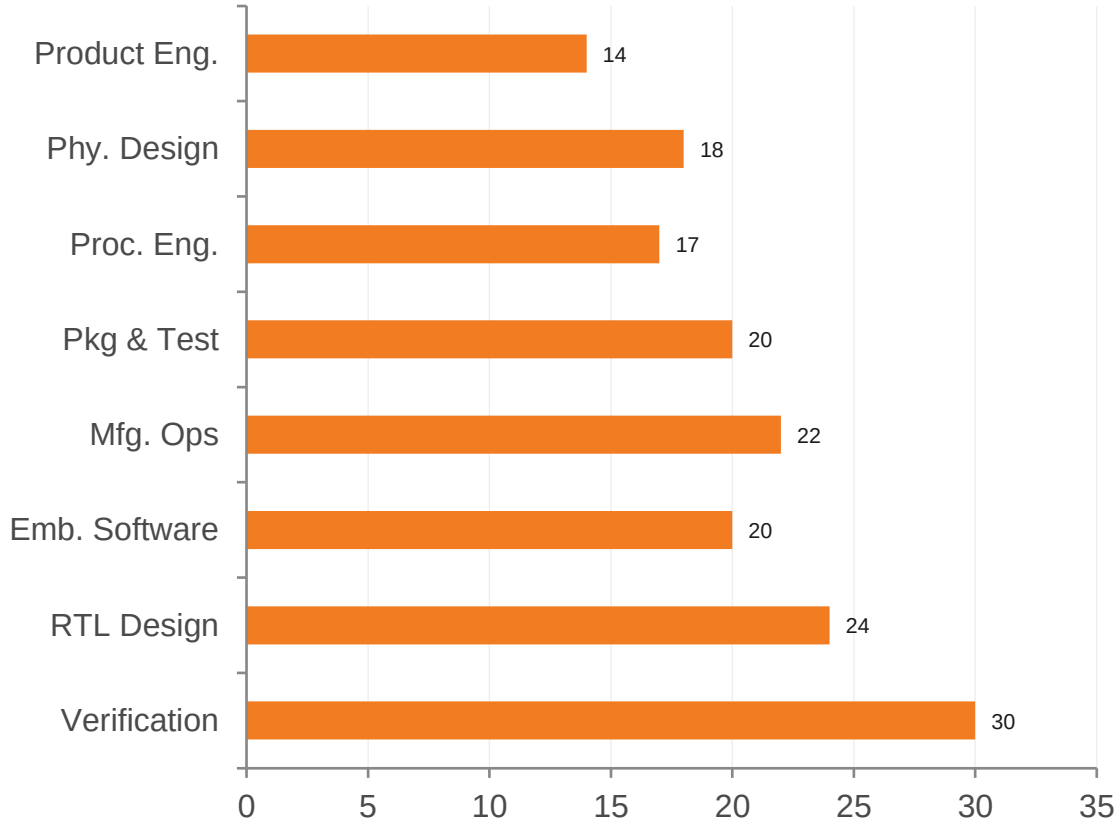
### SUPPLY CRUNCH — MID-SENIOR

CENTRAL STRATEGIC FINDING: 6–14 years experience band is critically scarce across all sub-industries — consistent across design, manufacturing, OSAT, and EDA. Process, yield, and verification leads have closure timelines of 16–30 weeks. This is the primary talent bottleneck for India's semiconductor ambitions.

### COMPENSATION PREMIUM

Design/GCC roles earn 25–35% above mainstream IT. Bengaluru +12–18%, Hyderabad +10–16% vs national semiconductor median. Highest premiums driven by AI/GPU/HPC demand (Nvidia, AMD, Qualcomm) and US–China tech-war diversification pulling senior design talent.

### WORKFORCE BY WORKSTREAM (EST.)




Sources: PIB ISM 2.0 (2026) · Careernet (2025–26) · India Briefing (2025) · Glassdoor (2026) | All estimated figures unless labeled DIRECT | DEMAND INTENT (investment/expansion announcements) vs ACTIVE HIRING (open roles/headcount adds) are distinct — see hiring market slides for labeling

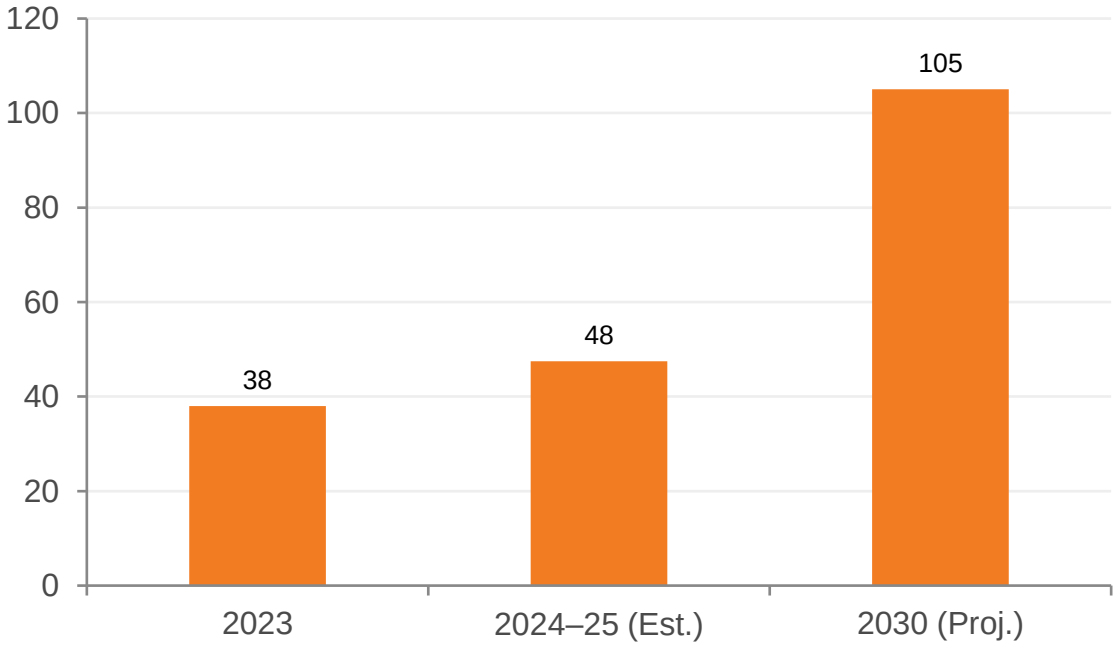
# 01

# INDUSTRY OVERVIEW

Market size · Workforce structure · Seniority pyramid · Talent concentration · Key drivers: AI Boom · US–China Tech War · Global Semiconductor Cycle · China+1

# INDUSTRY GROWTH & MARKET SIZE

## India Semiconductor Market (USD Billion)




[1] 2030 figure is government-projected via ISM 2.0. 2024–25 uses midpoint of $45–50B range.

## SUB-INDUSTRY GROWTH SIGNALS (2025–26)

| Sub-industry | Data basis | Hiring signal (2025–26) | Key drivers |
|---|---|---|---|
| **Chip Design / Fabless** | DIRECT policy priority | High | TOP DRIVERS: (1) AI Boom 2024–26 — explosive GPU/HPC/AI accelerator demand; Nvidia, AMD, Qualcomm driving hiring spikes; (2) US–China Tech War — chip design R&D shifting out of China, India benefiting in GCC design mandates; (3) GCC expansion + DLI (105 startups) |
| **Semiconductor Mfg. / Fabs** | DIRECT policy priority | High | Approved fabs: Gujarat, Assam moving to execution; China+1 supply-chain diversification driving backend (ATMP) investment — India gaining share vs Vietnam/Malaysia in packaging; advanced fab tech gap vs Taiwan/Korea remains |
| **OSAT / ATMP** | DIRECT policy priority | Very High | Micron, TSAT, CG Power ATMP units approved |
| **EDA & Semicon. Software** | Ecosystem relevance | High | EDA tool expansion, C2S design training |
| **Equip. & Materials** | DIRECT policy priority | High | ISM 2.0 explicitly targets domestic capability |
| **Embedded Semicon. Systems** | Scope-limited | Moderate | Only chip-linked embedded roles included |

~200,000–250,000 semiconductor professionals estimated in India (broad ecosystem estimate; 220,000 is one cited anchor within this range — India Briefing, 2025)

India hosts ~7% of global semiconductor GCCs and ~20% of global chip-design workforce

ISM 2.0 budget for FY26 approved; 3 semiconductor unit approvals in Gujarat + Assam | GLOBAL CYCLE: 2023 industry downturn → 2024–25 recovery led by AI/HPC → 2026 selective growth; India hiring mirrors this — AI/design roles recovering fastest, legacy/commodity roles lagging

Careernet: 3,549 GCC open roles in semiconductor design in Q1 FY2026 (ACTIVE HIRING); design GCC open positions fell 22% YoY in Q1 FY2026 vs Q1 FY2025, signaling post-2022–24 boom normalization, not a new boom

Sources: PIB ISM 2.0 (2026) · Careernet (2025–26) · India Briefing (2025)

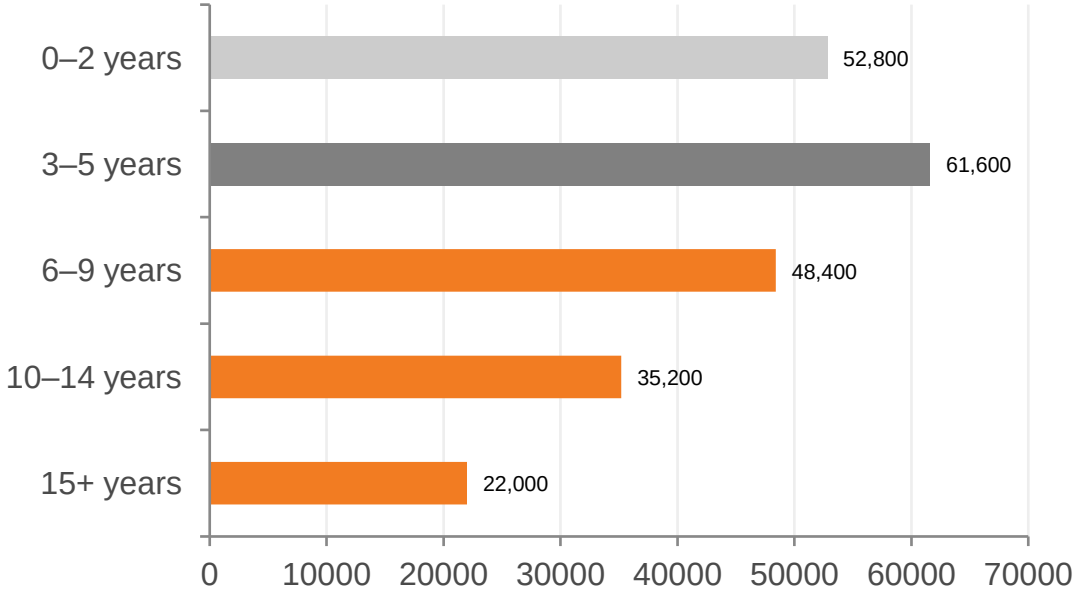
# WORKFORCE STRUCTURE — WORKSTREAM MIX

| Workstream | Est. Headcount | Share | Sub-industries | Primary Cities | Availability | Hiring Intensity |
|---|---|---|---|---|---|---|
| **RTL Design** | 24,000 | 11% | Chip Design / Fabless | Bengaluru, Hyderabad, Pune | Critical | High |
| **Physical Design** | 18,000 | 8% | Chip Design / Fabless | Bengaluru, Hyderabad, Chennai | Critical | High |
| **Verification & Validation** | 30,000 | 14% | Chip Design / Fabless, EDA | Bengaluru, Hyderabad, Chennai | Critical | High |
| **DFT** | 10,000 | 5% | Chip Design / Fabless | Bengaluru, Hyderabad, Pune | Low | High |
| **Analog / Mixed Signal** | 14,000 | 6% | Chip Design, Equipment | Bengaluru, Hyderabad, NCR | Low | Moderate |
| **Embedded Software / Firmware** | 20,000 | 9% | Design, System Software | Bengaluru, Hyderabad, Pune | Moderate | High |
| **Semiconductor Mfg. Operations** | 22,000 | 10% | Fabs, ATMP/OSAT | Gujarat, Assam, Chennai | Low | High |
| **Process Engineering** | 17,000 | 8% | Fabs, ATMP/OSAT | Gujarat, Assam, Chennai, NCR | Critical | High |
| **Packaging & Testing** | 20,000 | 9% | OSAT/ATMP | Gujarat, Assam, Chennai | Low | High |
| **EDA Tools & Automation** | 7,000 | 3% | EDA & Software | Bengaluru, Hyderabad, Pune | Moderate | Moderate |
| **Product Engineering** | 14,000 | 6% | Fabless, GCCs | Bengaluru, Hyderabad, NCR | Moderate | High |
| **Quality & Reliability** | 12,000 | 5% | Manufacturing, Packaging | Gujarat, Assam, Chennai, Bengaluru | Low | High |
| **Supply Chain & Procurement** | 11,000 | 5% | Manufacturing, OSAT | Gujarat, Chennai, NCR, Mumbai | Moderate | High |
| **Others (FAE, PM, Sales)** | 21,000 | 11% | Cross-functional | All metros | Moderate | Variable |
| **TOTAL** | ~220,000 (midpoint est.) | 100% | | | | |

All figures are estimates. Base: 200,000–250,000 estimated range (India Briefing 2025; 220,000 used as midpoint anchor). Allocation design-heavy per Careernet demand mix. Source: Careernet (2025–26), PIB ISM 2.0 (2026)

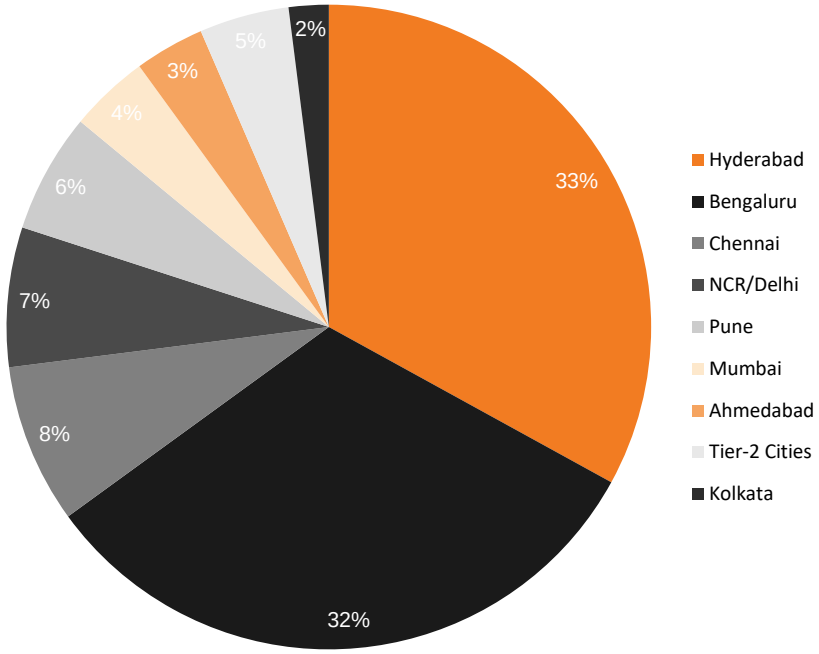
# SENIORITY PYRAMID & TALENT CONCENTRATION

## SENIORITY DISTRIBUTION (EST.)




| Band | Est. Headcount | Share | Supply Balance | Attrition Risk |
|---|---|---|---|---|
| **0–2 years** | 52,800 | 24% | Surplus-to-balanced | Moderate |
| **3–5 years** | 61,600 | 28% | Tight | High |
| **6–9 years** | 48,400 | 22% | SCARCE | High |
| **10–14 years** | 35,200 | 16% | CRITICAL | High |
| **15+ years** | 22,000 | 10% | Scarce | Moderate |

## CITY TALENT CONCENTRATION (EST.)




Design-led concentration: Bengaluru + Hyderabad = ~65% of design workforce. Manufacturing gravity shifting to Gujarat/Assam.

Design role mix (Careernet, FY2026): 48% core VLSI, 35% embedded/software, 17% business ops/IT. AI-led demand is concentrated in GPU/HPC/AI accelerator architecture, advanced verification, SoC/ASIC design, and compiler engineering — not across all design roles uniformly. Critical scarcity zone: 6–14 years across all design and manufacturing roles. Verification leads and process engineers are hardest to source.

Sources: Careernet (2025–26), PIB ISM 2.0 (2026), C2S/SMART pipeline data | All figures estimated

# 02

# COMPETITION MAPPING

Top employers · Functional dominance · City competition · Hiring intensity

# TOP EMPLOYERS BY SUB-INDUSTRY (2025–26)

| Sub-industry | Company | Type | Primary Cities | Core Focus | Seniority | Hiring Intensity | Momentum |
|---|---|---|---|---|---|---|---|
| **Chip Design / Fabless** | AMD | Global MNC | Bengaluru, Hyderabad | CPU/GPU, HPC, adaptive SoCs, verification | Mid-senior | Very High | High |
| **Chip Design / Fabless** | Qualcomm | Global MNC | Bengaluru, Hyderabad, Chennai | SoC, RF, AI on-device, mobile | Mid-senior | Very High | High |
| **Chip Design / Fabless** | Intel | Global MNC | Bengaluru, Hyderabad | RTL, validation, CPU, IP | Mid-senior | High | Moderate |
| **Chip Design / Fabless** | Nvidia | Global MNC | Bengaluru | GPU, AI silicon, verification | Mid-senior | Very High | High |
| **Chip Design / Fabless** | Texas Instruments | Global MNC | Bengaluru, NCR | Analog, embedded, design enablement | Mid-senior | High | High |
| **Semiconductor Mfg.** | Tata Electronics / TSAT | Indian Co. | Assam, Gujarat | Fab ops, packaging, process, quality | Mid-senior | Very High | High |
| **Semiconductor Mfg.** | Micron | Global MNC | Gujarat | ATMP, test, memory packaging | Mid-senior | Very High | High |
| **Semiconductor Mfg.** | CG Power–Renesas | Consortium | Gujarat | ATMP, test, manufacturing ops | Mid-senior | High | High |
| **OSAT / ATMP** | Micron | Global MNC | Gujarat | Packaging, test, quality | Mid-senior | Very High | High |
| **OSAT / ATMP** | TSAT | Indian Co. | Assam | Advanced packaging, flip-chip, SiP | Mid-senior | Very High | High |
| **EDA & Software** | Synopsys | Global MNC | Bengaluru, Hyderabad | EDA tool development, verification | Senior | High | High |
| **EDA & Software** | Cadence | Global MNC | Bengaluru, Hyderabad | Custom IC flows, tool engineering | Senior | High | High |
| **Equip. & Materials** | Applied Materials | Global MNC | Bengaluru, Chennai | Equipment engineering, apps | Mid-senior | High | High |
| **Equip. & Materials** | Lam Research | Global MNC | Bengaluru, Chennai | Tool engineering, process support | Mid-senior | High | High |

Sources: PIB ISM 2.0 (2026) · ET CIO (2024) · ET GCC (2026) · Times of India (2024) | Headcount estimates are proxy-based where marked NA in source data | CHINA+1 NOTE: India's GCC expansion reflects design-capability pull and policy incentives. Work shifting from China to India at named-company scale is a directional hypothesis; company-level case studies needed to confirm. India's strength is design/GCC; advanced fab capability gaps vs Taiwan/Korea remain.

# FUNCTIONAL DOMINANCE & COMPETITION HEATMAP

## FUNCTION × COMPETITION INTENSITY

| Function | Dominant Cities | Key Employers | Competition | Scarcity |
|---|---|---|---|---|
| **RTL Design** | Bengaluru, Hyderabad | AMD, Intel, Qualcomm, TI, Nvidia | Very High | Critical |
| **Physical Design** | Bengaluru, Hyderabad, Chennai | AMD, Intel, Qualcomm, Synopsys | Very High | Critical |
| **Verification** | Bengaluru, Hyderabad, Chennai | AMD, Intel, Qualcomm, Nvidia, TI | EXTREME | Critical |
| **DFT** | Bengaluru, Hyderabad, Pune | Intel, AMD, Qualcomm, startups | High | High |
| **Analog / Mixed Signal** | Bengaluru, NCR, Hyderabad | TI, NXP, Infineon, Renesas | High | High |
| **Embedded Software** | Bengaluru, Hyderabad, Pune | Qualcomm, Nvidia, AMD, TI | Very High | High |
| **Process Engineering** | Gujarat, Assam, Chennai | TSAT, Micron, PSMC, OEMs | EXTREME | Critical |
| **Yield Engineering** | Gujarat, Assam | Micron, TSAT | EXTREME | Critical |
| **Packaging & Testing** | Gujarat, Assam, Chennai | Micron, TSAT, CG Power | High | Critical |
| **EDA Tool Development** | Bengaluru, Pune, Hyderabad | Synopsys, Cadence, Siemens EDA | High | High |
| **HPC / CPU / GPU** | Bengaluru, Hyderabad | AMD, Intel, Nvidia | EXTREME | Critical |
| **RF / Wireless** | Bengaluru, Hyderabad | Qualcomm, TI, Nvidia | Very High | Critical |

## HIRING COMPETITION HEATMAP (SUB-INDUSTRY × CITY)

| Sub-industry | Bengaluru | Hyderabad | Chennai | Pune | Ahmedabad | NCR |
|---|---|---|---|---|---|---|
| **Chip Design** | Extreme | Extreme | High | High | High | Moderate |
| **Mfg. / Fabs** | Moderate | Moderate | Moderate | Low | High (Gujarat) | Low |
| **OSAT / ATMP** | Moderate | Moderate | High | Low | High (Gujarat) | Low |
| **EDA & Software** | Extreme | Extreme | Moderate | Moderate | Low | Low |
| **Equip. & Materials** | High | Moderate | High | Moderate | Moderate | Low |

## EMPLOYER EXPANSION MOMENTUM

| Company | Expansion signal | Hiring impact |
|---|---|---|
| **Texas Instruments** | New 550,000 sq.ft. R&D facility, Bengaluru | Very High |
| **Micron** | ATMP/fab ecosystem buildout, Gujarat | Very High |
| **TSAT** | Fab + ATMP execution, Assam & Gujarat | Very High |
| **AMD** | 3,000-engineer campus plan, Bengaluru | High |
| **CG Power–Renesas** | New ATMP unit, Gujarat | High |
| **Design GCCs (sector)** | 3,549 active open roles Mar 2026 (partial recovery from 2025 trough; down 22% vs Q1 FY2025) | High |

Sources: ET GCC (2026) · PIB ISM 2.0 (2026) · Times of India (2024) · Careernet (2025–26) · ET CIO (2024)

# 03

# TALENT ARCHITECTURE

City talent pools · Cluster mapping · Campus hiring · Talent gap analysis

# CITY TALENT POOLS BY SUB-INDUSTRY (EST.)

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## CHIP DESIGN / FABLESS

| City | Est. Pool | Share | Key Functions | Availability | Comp. Pressure |
|---|---|---|---|---|---|
| **Bengaluru** | 32,000 | 32% | RTL, Verif., PD | Low | Very High |
| **Hyderabad** | 27,000 | 27% | RTL, Verif., PD, SW | Low | Very High |
| **Chennai** | 10,000 | 10% | Verif., Embedded | Moderate | High |
| **Pune** | 7,000 | 7% | PD, Embedded, PE | Moderate | High |
| **NCR/Delhi** | 6,000 | 6% | Product, PM, SW | Moderate | High |
| **Tier-2 Cities** | 10,000 | 10% | Junior Design, Support | Moderate | Moderate |
| **Others** | 8,000 | 8% | Mixed | Moderate | Moderate |

## EDA & SEMICONDUCTOR SOFTWARE

| City | Est. Pool | Share | Key Functions | Availability | Comp. Pressure |
|---|---|---|---|---|---|
| **Bengaluru** | 18,000 | 45% | EDA dev, Automation | Low | Very High |
| **Hyderabad** | 9,000 | 22.5% | EDA flows, SW | Low | Very High |
| **Pune** | 4,000 | 10% | Tools, Automation | Moderate | High |
| **Tier-2 Cities** | 5,200 | 13% | Junior tooling, SW | Moderate | Moderate |
| **Chennai** | 2,000 | 5% | Verif. tools | Moderate | High |

## SEMICONDUCTOR MANUFACTURING / FABS

| City | Est. Pool | Share | Key Functions | Availability | Comp. Pressure |
|---|---|---|---|---|---|
| **Gujarat cluster** | 9,000 | 45% | Process, Yield, Mfg. Ops | Low | High |
| **Chennai** | 3,000 | 15% | Process support, Quality | Low | High |
| **Tier-2 Cities** | 7,500 | 37.5% | Mfg. ops, Technician | Moderate | Moderate |
| **Bengaluru** | 2,000 | 10% | Process R&D, Equip. apps | Moderate | Very High |

## SEMICONDUCTOR EQUIPMENT & MATERIALS

| City | Est. Pool | Share | Key Functions | Availability | Comp. Pressure |
|---|---|---|---|---|---|
| **Tier-2 Cities** | 7,200 | 36% | Service, Technician | Moderate | Moderate |
| **Bengaluru** | 5,000 | 25% | Apps Eng., Field Svc. | Low | High |
| **Chennai** | 4,000 | 20% | Apps, Service, Process | Low | High |
| **Pune** | 2,500 | 12.5% | Field service, Tooling | Moderate | High |
| **Ahmedabad** | 1,000 | 5% | Process support, Materials | Moderate | High |

Sources: PIB ISM 2.0 (2026) · Careernet via Moneycontrol (2026) · Xpheno (2026) | All pool sizes are estimates

# TALENT GAP ANALYSIS — CRITICAL ROLES

*Gap Severity: Low = manageable | Moderate = visible constraints | High = significant scarcity | Critical = severe shortage, 16+ week closures*

| Role | City | Exp. Band | Supply | Demand | Gap | Difficulty | Closure | Comp. Pressure | Key Cause |
|---|---|---|---|---|---|---|---|---|---|
| **Verification** | Bengaluru | 3–5 yrs | High | Very High | High | Hard | 8–14 wks | Very High | High role concentration across GCCs |
| **Verification** | Hyderabad | 6–9 yrs | Medium | Very High | CRITICAL | Very Hard | 12–20 wks | Extreme | Senior ownership scarce |
| **Physical Design** | Bengaluru | 6–9 yrs | Medium | High | High | Hard | 10–16 wks | Very High | Small specialist pool |
| **RTL Design** | Hyderabad | 10–14 yrs | Low-Med | High | CRITICAL | Very Hard | 12–24 wks | Extreme | Leadership depth limited |
| **Analog / Mixed Signal** | NCR | 6–9 yrs | Low | Medium | CRITICAL | Very Hard | 12–24 wks | Extreme | Few qualified candidates |
| **Process Engineering** | Gujarat | 3–5 yrs | Low | Very High | CRITICAL | Very Hard | 16–26 wks | Extreme | New fab ramp, low local depth |
| **Yield Engineering** | Gujarat | 6–9 yrs | Very Low | High | CRITICAL | Very Hard | 20–30 wks | Extreme | Very limited India bench |
| **Packaging & Testing** | Gujarat | 3–5 yrs | Low | Very High | CRITICAL | Very Hard | 16–24 wks | High | New ATMP scale-up |
| **Packaging & Testing** | Gujarat | 6–9 yrs | Low | Very High | CRITICAL | Very Hard | 16–28 wks | Extreme | Senior packaging engineers scarce |
| **Quality & Reliability** | Chennai | 6–9 yrs | Low-Med | High | High | Hard | 12–18 wks | High | Cross-over supply limited |
| **Test Engineering** | Ahmedabad | 3–5 yrs | Low | High | High | Hard | 12–20 wks | High | New ecosystem |
| **Mfg. Operations** | Assam | 0–2 yrs | Medium | High | Moderate | Moderate | 6–12 wks | Moderate | Trainable pool available |

Sources: Careernet (2025–26) · InvestmentGuruIndia (2025) · PIB ISM 2.0 (2026) | Closure timelines and severity are proxy-estimated — directional only

# CAMPUS HIRING LANDSCAPE & SCARCITY HEATMAPS

## CAMPUS SEMICONDUCTOR PIPELINE

| Institute | Semicon. Output | Key Sub-industries | Hiring Intensity | Notes |
|---|---|---|---|---|
| **IITs** | High | Design, EDA, Product Eng. | Very High | Targeted specialist hiring |
| **IISc** | Med-High | Design, Advanced R&D | Very High | Strong research-to-industry link |
| **Top NITs** | Medium | Design, Embedded, Test | High | Good volume + quality |
| **IIITs** | Medium | Embedded, Verif., SW | High | Strong applied projects |
| **VLSI-specific institutes** | Medium | VLSI, Verif., Embedded | High | Useful for fresher sourcing |
| **Regional engineering** | Medium | Mfg. support, Test, QA | Moderate | Ops roles pipeline |

Most targeted campus skills: verification, embedded firmware, analog/mixed-signal, board validation, design/IP. GCCs more campus-active for design & software; Indian manufacturers prefer process/quality graduates with internship exposure.

## SCARCITY HEATMAP — CITY × ROLE TYPE

| City | Design | Manufacturing | OSAT | EDA | Equipment |
|---|---|---|---|---|---|
| **Bengaluru** | High | Moderate | Moderate | High | High |
| **Hyderabad** | High | Moderate | Moderate | High | Moderate |
| **Chennai** | Moderate | High | High | Moderate | High |
| **Pune** | Moderate | Low-Med | Low-Med | Moderate | Moderate |
| **NCR / Delhi** | Moderate | Low | Low | Moderate | Low |
| **Ahmedabad** | Low-Med | CRITICAL | CRITICAL | Low | Moderate |
| **Tier-2 Cities** | Moderate | High | High | Low | High |

## SCARCITY HEATMAP — EXPERIENCE × FUNCTION

| Exp. Band | Design | Manufacturing | OSAT | EDA | Equipment |
|---|---|---|---|---|---|
| **0–2 years** | Moderate | Moderate | Moderate | Moderate | Moderate |
| **3–5 years** | High | High | High | High | High |
| **6–9 years** | CRITICAL | CRITICAL | CRITICAL | High | High |
| **10–14 years** | CRITICAL | CRITICAL | CRITICAL | CRITICAL | High |
| **15+ years** | High | High | High | High | High |

Sources: Economic Times (2025) · IISc admissions (2026) · Careernet (2025) · PIB (2026) | Scarcity classifications are derived/proxy-based

# 04

# COMPENSATION

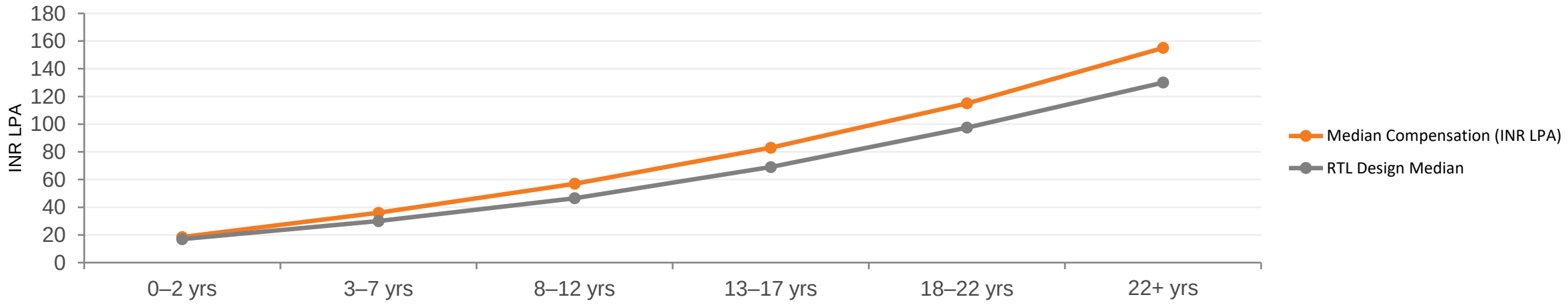
Role × experience matrices · Sub-industry premiums · City & skill premiums

# COMPENSATION MATRIX — CHIP DESIGN / FABLESS (INR LPA)

*Annual fixed compensation ranges (INR Lakhs per annum). Does not include stock/ESOP unless implicit in senior bands. Source: Taggd (2025), Zinnov GCC (2025), Levels.fyi (2026) — estimated.*

| Role | 0–2 yrs | 3–7 yrs | 8–12 yrs | 13–17 yrs | 18–22 yrs | 22+ yrs |
|---|---|---|---|---|---|---|
| **RTL Design Engineer** | 14–20 | 24–36 | 38–55 | 58–80 | 85–110 | 110–150 |
| **Physical Design Engineer** | 15–22 | 28–42 | 45–65 | 68–92 | 95–125 | 125–170 |
| **Verification Engineer** | 15–22 | 28–44 | 46–68 | 70–96 | 100–130 | 130–180 |
| **DFT Engineer** | 14–20 | 24–38 | 40–60 | 62–84 | 88–115 | 115–155 |
| **Analog Design Engineer** | 16–24 | 30–46 | 48–72 | 75–100 | 105–140 | 140–190 |
| **SoC Architect** | NA | NA | 70–100 | 100–140 | 140–190 | 190–260 |
| **Firmware Engineer** | 12–18 | 20–32 | 34–50 | 52–72 | 75–100 | 100–135 |

**VERIFICATION ENGINEER — MEDIAN COMPENSATION TREND (INR LPA)**




Sources: Taggd (2025) · Zinnov GCC Salary Report (2025) · Levels.fyi (2026) | Ranges are estimated — sensitivity high to employer type and location

# COMPENSATION MATRICES — MANUFACTURING · OSAT · EDA · EQUIPMENT (INR LPA)

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## SEMICONDUCTOR MANUFACTURING / FABS

| Role | 0–2 | 3–7 | 8–12 | 13–17 | 18–22 | 22+ |
|---|---|---|---|---|---|---|
| **Process Engineer** | 10–16 | 18–30 | 32–48 | 50–72 | 75–100 | 100–140 |
| **Yield Engineer** | NA | 20–32 | 35–52 | 55–78 | 80–110 | 110–155 |
| **Equipment Engineer** | 9–14 | 16–26 | 28–42 | 44–64 | 66–92 | 92–125 |
| **Manufacturing Operations** | 8–12 | 14–22 | 24–36 | 38–54 | 56–78 | 78–110 |
| **Fab Automation Engineer** | 12–18 | 22–34 | 36–55 | 58–82 | 85–115 | 115–160 |

## OSAT / ATMP

| Role | 0–2 | 3–7 | 8–12 | 13–17 | 18–22 | 22+ |
|---|---|---|---|---|---|---|
| **Packaging Engineer** | 10–15 | 18–28 | 30–45 | 48–68 | 70–95 | 95–130 |
| **Test Engineer** | 10–15 | 18–28 | 30–46 | 48–70 | 72–98 | 98–135 |
| **Reliability Engineer** | 10–16 | 18–30 | 32–48 | 50–72 | 75–100 | 100–140 |
| **Product Engineer** | 12–18 | 22–34 | 36–55 | 58–82 | 85–115 | 115–160 |
| **Failure Analysis Eng.** | NA | 20–32 | 34–50 | 52–75 | 78–105 | 105–145 |

## EDA & SEMICONDUCTOR SOFTWARE

| Role | 0–2 | 3–7 | 8–12 | 13–17 | 18–22 | 22+ |
|---|---|---|---|---|---|---|
| **EDA Software Developer** | 14–22 | 26–40 | 42–62 | 65–90 | 95–125 | 125–170 |
| **CAD Automation Engineer** | 13–20 | 24–36 | 38–56 | 58–82 | 85–110 | 110–150 |
| **Compiler Engineer** | 16–24 | 30–46 | 48–72 | 75–105 | 110–145 | 145–195 |
| **AI/ML Semicon. Engineer** | NA | 30–48 | 52–80 | 85–120 | 125–165 | 165–220 |

## SEMICONDUCTOR EQUIPMENT & MATERIALS

| Role | 0–2 | 3–7 | 8–12 | 13–17 | 18–22 | 22+ |
|---|---|---|---|---|---|---|
| **Field Applications Engineer** | 12–18 | 22–34 | 36–55 | 58–82 | 85–115 | 115–155 |
| **Process Integration Engineer** | 13–20 | 24–36 | 38–58 | 60–86 | 88–120 | 120–165 |
| **Equipment Support Engineer** | 10–16 | 18–28 | 30–46 | 48–68 | 70–95 | 95–130 |
| **Materials Specialist** | 12–18 | 22–34 | 36–54 | 56–80 | 82–110 | 110–150 |

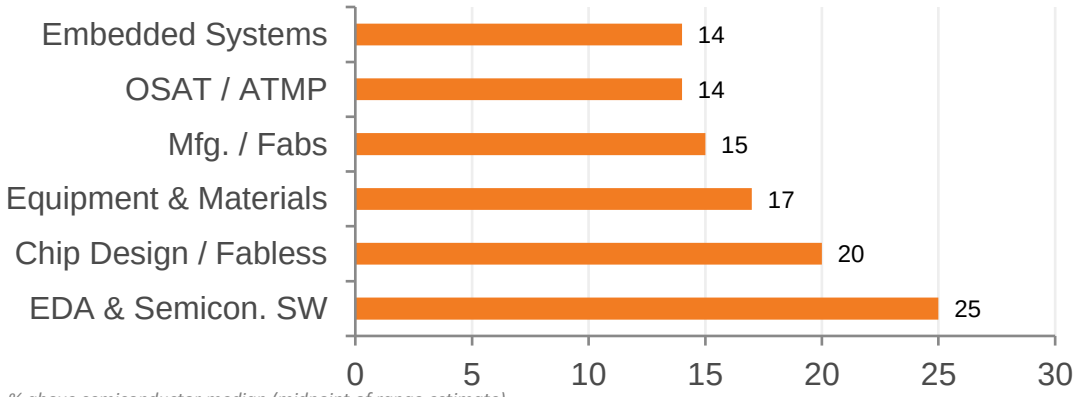
## EMBEDDED SEMICONDUCTOR SYSTEMS

| Role | 0–2 | 3–7 | 8–12 | 13–17 | 18–22 | 22+ |
|---|---|---|---|---|---|---|
| **Embedded Firmware Engineer** | 12–18 | 20–32 | 34–50 | 52–72 | 75–100 | 100–135 |
| **Automotive Embedded Engineer** | 13–20 | 24–36 | 38–58 | 60–85 | 88–120 | 120–160 |
| **Edge AI Engineer** | 16–24 | 30–46 | 48–72 | 75–105 | 110–145 | 145–195 |

Sources: Taggd (2025) · Zinnov GCC Report (2025) · Levels.fyi (2026) | All figures estimated — confidence Low–Moderate | Ranges are annual fixed; no stock/ESOP included

# SUB-INDUSTRY, CITY & SKILL PREMIUM ANALYSIS

### SUB-INDUSTRY PREMIUM vs. SEMICONDUCTOR MEDIAN

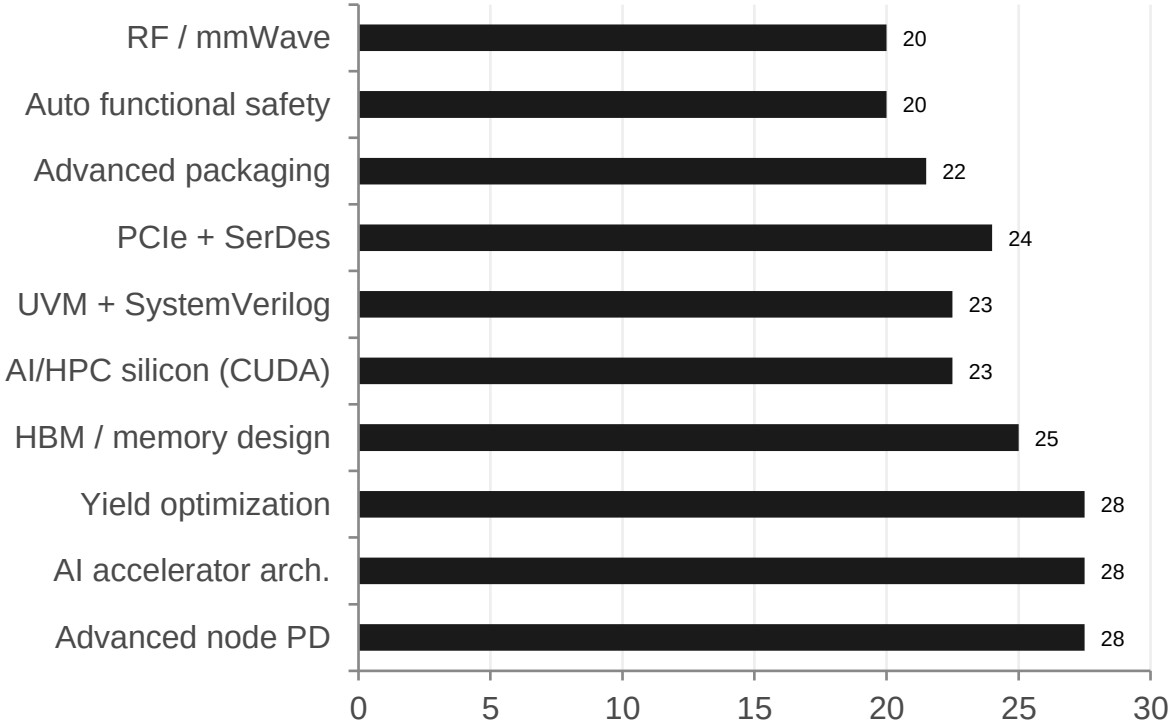



*% above semiconductor median (midpoint of range estimate)*

### CITY PREMIUM / DISCOUNT vs. SEMICONDUCTOR MEDIAN

| City | Premium vs. Median | Cost Competitiveness | Comp. Inflation Risk | Key Driver |
|---|---|---|---|---|
| **Bengaluru** | +12–18% | Very High | Extreme | Scarcity + GCC density |
| **Hyderabad** | +10–16% | Very High | Extreme | Scarcity + GCC density |
| **NCR / Delhi** | +5–12% | Moderate | High | Leadership + HQ premium |
| **Chennai** | +4–10% | Medium | High | Process + quality roles |
| **Mumbai** | +3–8% | Medium | Moderate | Commercial/leadership |
| **Pune** | +2–8% | Medium | Moderate | EDA + embedded niche |
| **Ahmedabad** | -3% to +4% | High | Rising | Emerging mfg. market |
| **Tier-2 Cities** | -5% to -12% | Very High | Moderate | Cost arbitrage |

### TOP SKILL PREMIUMS (ESTIMATED %)




*% above base role compensation (midpoint estimates). Strongest at 8–22 year experience bands.*

Sources: Taggd (2025) · InvestmentGuruIndia (2025) · PIB ISM 2.0 (2026) | Premiums are proxy-based estimates — confidence Low–Moderate

# 05

# WORKFORCE BEHAVIOUR

Attrition · Switching intent · City mobility · Retention risks

# ATTRITION LANDSCAPE — BY SUB-INDUSTRY & ROLE

*No public India semiconductor attrition census exists. All figures are derived proxy estimates based on GCC hiring volatility, role scarcity, and staffing commentary.*

### ATTRITION BY SUB-INDUSTRY

| Sub-industry | Attrition Rate | Trend | Comp. Sensitivity | Leadership Stability |
|---|---|---|---|---|
| **Chip Design / Fabless** | High | Rising→Stabilizing | Very High | Moderate |
| **EDA & Semicon. Software** | High | Rising | Very High | High |
| **OSAT / ATMP** | Moderate-High | Rising | High | Moderate |
| **Semicon. Mfg. / Fabs** | Moderate | Rising | High | Moderate |
| **Equipment & Materials** | Moderate | Stable-Rising | Moderate-High | High |
| **Embedded Semicon. Systems** | Moderate | Stable | Moderate | Moderate |

### ATTRITION BY EXPERIENCE BAND

| Exp. Band | Attrition Rate | Primary Drivers | Retention Complexity |
|---|---|---|---|
| **0–2 years** | Moderate-High | First-job churn, mismatch | Moderate |
| **3–7 years** | High | Pay jumps, brand switching | High |
| **8–12 years** | VERY HIGH | Scarcity-driven poaching, role progression | CRITICAL |
| **13–17 years** | High | Leadership opp., counteroffers | Critical |
| **18–22 years** | Moderate | Selective moves, executive pull | High |
| **22+ years** | Moderate | Strategic lateral moves | High |

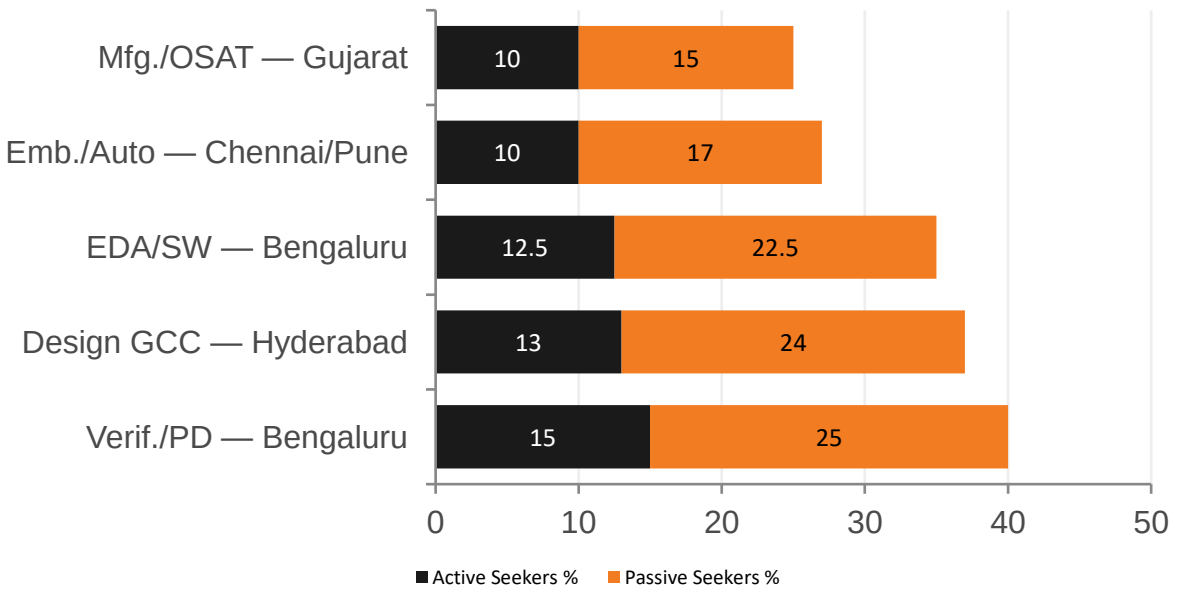
### ATTRITION BY ROLE

| Role | Attrition Rate | Trend | Poaching Intensity | Retention Risk |
|---|---|---|---|---|
| **Verification** | VERY HIGH | Rising | Extreme | CRITICAL |
| **Physical Design** | High | Rising | Very High | High |
| **RTL Design** | High | Rising | High | High |
| **Process Engineering** | High | Rising | Very High | CRITICAL |
| **Yield Engineering** | High | Rising | Very High | CRITICAL |
| **EDA Development** | High | Rising | Very High | High |
| **Embedded Software** | High | Rising | High | High |
| **Product Engineering** | High | Rising | High | High |
| **Packaging & Testing** | Moderate-High | Rising | High | High |
| **DFT** | High | Rising | High | High |
| **Manufacturing Ops** | Moderate | Rising | Moderate | Moderate-High |
| **Supply Chain** | Moderate | Stable | Moderate | Moderate |

Sources: HRKatha citing Careernet (2026) · Taggd (2026) · PIB ISM 2.0 (2026) | All attrition figures are derived proxy estimates | HIRING CYCLE CONTEXT: 2022–24 was a strong GCC expansion boom; 2025 saw normalization (−22% YoY open roles in design GCCs); 2026 shows partial recovery (3,549 active roles). Recovery is skill-specific, not uniformly broad-based.

# SWITCHING INTENT & CITY MOBILITY

## JOB CHANGE INTENT BY SEGMENT (PROXY ESTIMATE)




*Active = currently interviewing. Passive = open to explore. Midpoints used.*

## CITY WORKFORCE MOBILITY MATRIX

| City | Attrition Level | Considering Change | Hiring Competition | Comp. Inflation | Expansion Attr. |
|---|---|---|---|---|---|
| **Bengaluru** | High | 30–40% | Extreme | Very High | Low |
| **Hyderabad** | High | 28–38% | Extreme | Very High | Low |
| **Chennai** | Moderate-High | 22–32% | High | High | Moderate |
| **Pune** | Moderate | 18–28% | High | Moderate | Moderate |
| **NCR / Delhi** | Moderate | 18–28% | High | High | Moderate |
| **Ahmedabad** | Moderate | 12–22% | High | Moderate | Very High |
| **Mumbai** | Moderate | 15–25% | Moderate | High | Moderate |
| **Tier-2 Cities** | Moderate | 12–22% | Moderate | Low-Mod. | High |
| **Kolkata** | Low-Moderate | 10–18% | Low | Low | Low |

## RETENTION RISK HEATMAP

| Layer | LOW | MODERATE | HIGH | CRITICAL |
|---|---|---|---|---|
| **Role level** | FPGA, Supply Chain | Mfg. Ops, Apps Eng. | RTL, PD, Embedded, Packaging | Verification, Process, Yield, EDA |
| **City level** | Kolkata | Pune, Mumbai | Chennai, Ahmedabad | Bengaluru, Hyderabad |
| **Sub-industry** | Equipment / Materials | Mfg. / Fabs | OSAT / ATMP | Chip Design / Fabless, EDA |

Sources: HRKatha citing Careernet (2026) · Taggd (2026) · Deloitte Semiconductor Outlook (2025) | All mobility and intent figures are proxy-estimated | GCC vs INDIAN EMPLOYER NOTE: GCCs (AMD, Qualcomm, Nvidia, TI) tend to offer higher comp, stronger brand pull, and global mobility — driving higher switching risk from Indian employers. Indian fabs/ATMP (TSAT, Micron India) benefit from scarcity of alternatives locally but face steeper mid-senior retention pressure as GCC demand grows.

# Get in touch

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